 **East West University**

**Project Report**

**Semester:** Summer-2025

**Course Title:** Electrical Circuits **Course Code:** CSE209

**Sec:** 01

**Group No: 05**

**Group Members:**

|  |  |
| --- | --- |
| **Student Name** | **Student Id** |
| **Md. Arifur Rahman Razu** | **2024-3-60-503** |
| **Zahin Abdullah Adib** | **2024-1-60-164** |
| **Purnima Ghosh** | **2023-3-60-522** |
| **Nusrat Jahan Fiha** | **2023-2-60-137** |

**Submitted by-**

Name: Md. Arifur Rahman Razu

ID: 2024-3-60-503

**Submitted to-**

Dr. Sarwar Jahan

Associate Professor

Department of Computer Science & Engineering

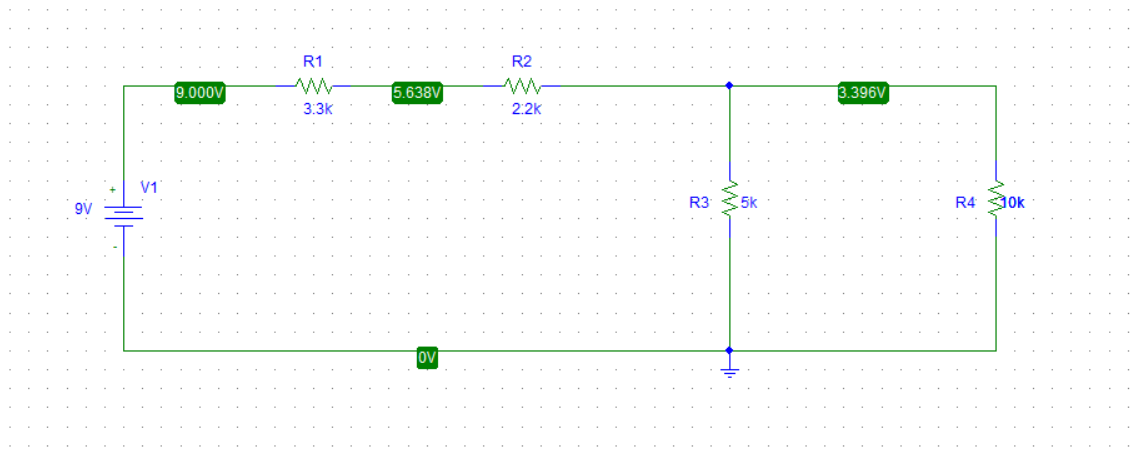
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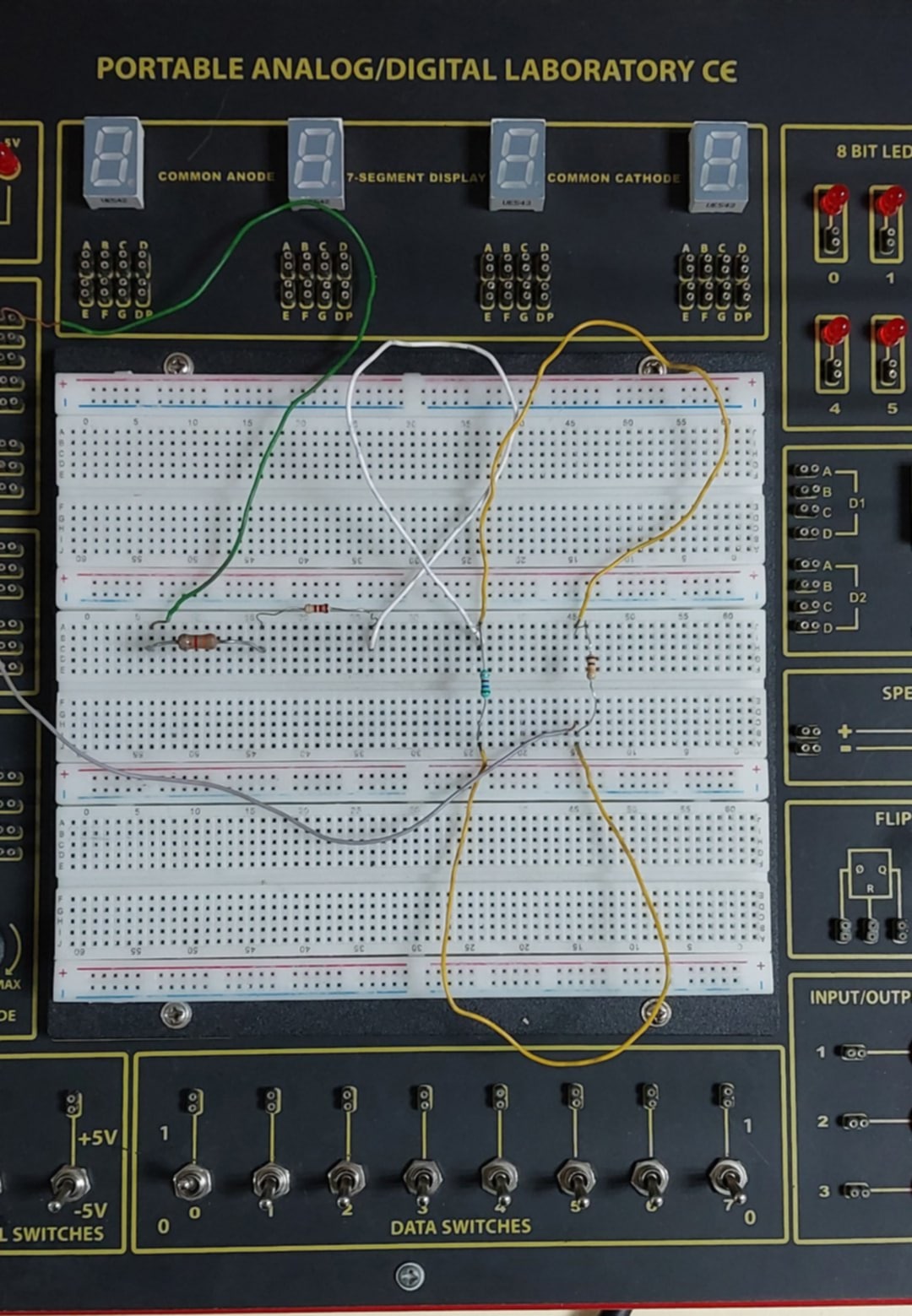
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**1. Introduction**

The objective of this project is to design and implement a multi-stage resistor network with both series and parallel configurations. The designed circuit ensures that the voltage is properly distributed across resistors in series-parallel combinations, and the sum of individual voltage drops equals the total source voltage. The project includes theoretical analysis, simulation, practical implementation, and measurement comparison.

**2. Circuit Design**

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The circuit consists of:

* A DC voltage source of **9V**
* Four resistors:
  + R1=3.3 kΩ
  + R2=2.2 kΩ
  + R3=5 kΩ
  + R4=10 kΩ

**Configuration:**

* R1​ and R2​ are connected in series.
* The combination of R3​ and R4​ in parallel is connected after them, forming a mixed series-parallel circuit.

A labeled circuit diagram was constructed both in PSpice and on a breadboard.

**3. Theoretical Calculations**

**Equivalent Resistance**

R3||R4 = R3×R4/R3+R4 = 5×10/5+10 = 3.33 kΩ

Req = R1+R2+R34 = 3.3+2.2+3.33 = 8.8 kΩ

**Total Current**

I=V/Req = 98.8 = 1.02 mA

**Voltage Drops**

* Across R1​:

V1 = I×R1 = 1.02×3.3 = 3.366 V

* Across R2:

V2 = I×R2 = 1.02×2.2 = 2.244 V

* Across parallel branch (R3 and R4​):

I’ = 1.02×5/15 = 0.34 mA

V3 = V4 = I′×R3 = 3.4 V

**4. Practical Measurements**

Using a breadboard setup with the given resistors and a DC power supply, the following values were obtained:

* V1=3.306 V
* V2=2.122 V
* V3=3.561 V

**5. Results and Comparison**

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Theoretical (V)** | **Practical (V)** |
| **V1** | **3.366** | **3.306** |
| **V2** | **2.244** | **2.122** |
| **V3** | **3.4** | **3.561** |

**Observation:** The practical results are very close to the theoretical ones, with small deviations due to:

* Resistor tolerance.
* Internal resistance of the power source.
* Breadboard connection losses.

**6. Discussion and Error Analysis**

* The difference between theoretical and measured results is within acceptable range.
* Errors mainly arise from resistor tolerance values and measurement inaccuracies.
* Simulation results (PSpice) closely matched theoretical calculations, confirming design correctness.
* Practical implementation validates the theoretical model with minor variations.

**7. Conclusion**

The project successfully demonstrated a series-parallel resistor network. The calculated and measured voltage values matched well, confirming Ohm’s Law and Kirchhoff’s Voltage Law (KVL). The experiment highlights the importance of tolerance in circuit design and provides insights into practical implementation differences compared to theoretical predictions.